

ISSUE CLASSIFICATION	
Class	Subclass

PATENT NUMBER

<p>O.I.P.E.</p> <p>SCANNED <i>[Signature]</i> O.A. <i>[Signature]</i></p>	<p>PATENT DATE</p>
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APPLICATION NO. 09/926202	CONT/PRIOR D F	CLASS 117	SUBCLASS C	ART UNIT 1765	EXAMINER /111 111
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Hiroshi Takeno

Method for producing silicon epitaxial wafer

PTO-2040
12/89[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS		CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)		NOTICE OF ALLOWANCE MAILED	
	_____ (Primary Examiner) (Date)		ISSUE FEE	
Amount Due			Date Paid	
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<input type="checkbox"/> The terminal ____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) (Date)		ISSUE BATCH NUMBER	

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